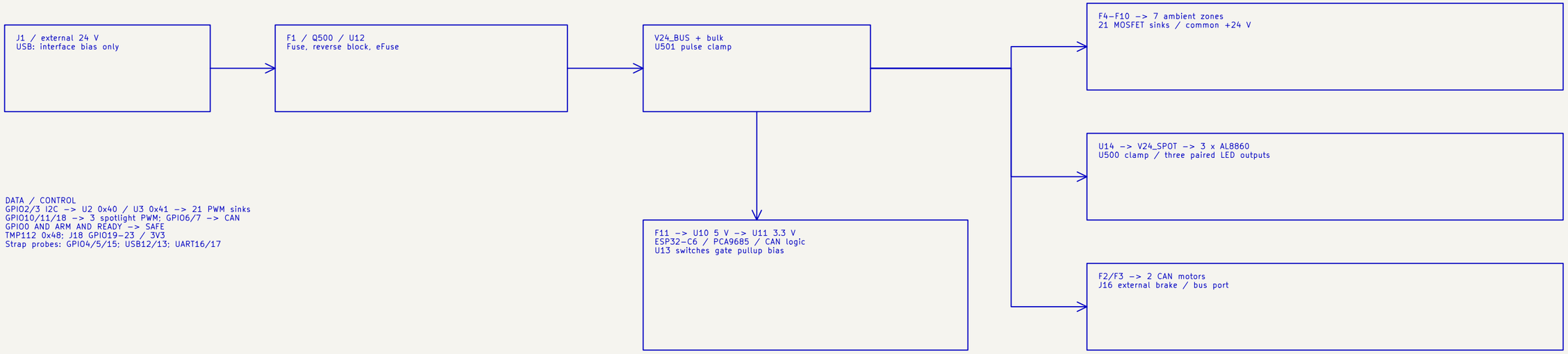
76.2 mm envelope / eight copper layers / factory SMD assembly
Functional energy and data map — electrical nets are on the child sheets.



DATA / CONTROL
GPIO2/3 I2C –> U2 0x40 / U3 0x41 –> 21 PWM sinks
GPIO10/11/18 –> 3 spotlight PWM; GPIO6/7 –> CAN
GPIO0 AND ARM AND READY –> SAFE
TMP112 0x48; J18 GPIO19–23 / 3V3
Strap probes: GPIO4/5/15; USB12/13; UART16/17

Prototype only: source/current/thermal/RF and motor-energy tests remain pending.
Open ARM = lighting inhibited. Motor stopping/holding is a separate function.

controller
File: controller.kicad_sch

power_sequence
File: power_sequence.kicad_sch

can
File: can.kicad_sch

usb
File: usb.kicad_sch

pwm
File: pwm.kicad_sch

zone_1
File: zone_1.kicad_sch

zone_2
File: zone_2.kicad_sch

zone_3
File: zone_3.kicad_sch

zone_4
File: zone_4.kicad_sch

zone_5
File: zone_5.kicad_sch

zone_6
File: zone_6.kicad_sch

zone_7
File: zone_7.kicad_sch

test
File: test.kicad_sch

power_1
File: power_1.kicad_sch

power_2
File: power_2.kicad_sch

spot_1
File: spot_1.kicad_sch

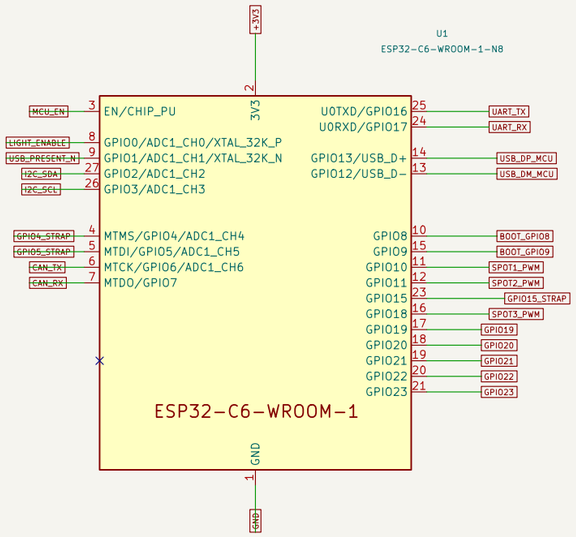
spot_2
File: spot_2.kicad_sch

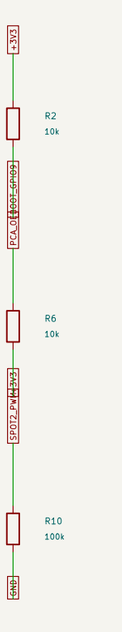
monitor_expansion
File: monitor_expansion.kicad_sch

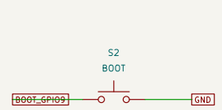
central_led_interface
File: central_led_interface.kicad_sch

ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting
Sheet: /
File: engineered-lighting-rev-a.kicad_sch
Title: Integrated lighting controller
Size: A3 | Date: 2026-09-08 | **Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3 | Id: 1/20

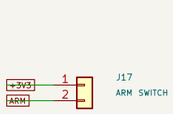
CONTROLLER

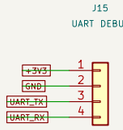


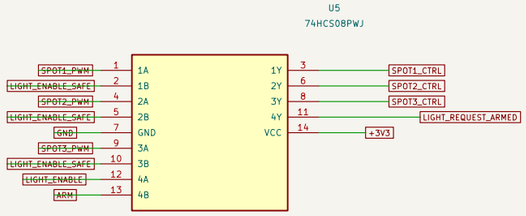


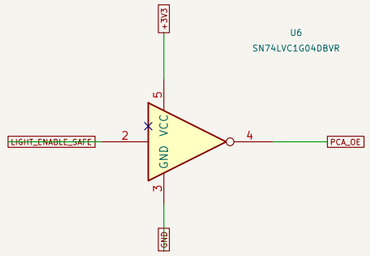


GPIO 0 AND physical ARM -> LIGHT_REQUEST_ARMED
U19 on power_sequence adds READY qualification -> LIGHT_ENABLE_SAFE.
MCU_EN reset remains here; U18 reaches it through current-limiting R42.









ENGINEERING DRAFT — see release status before fabrication

Engineered Lighting

Sheet: /controller/
File: controller.kicad_sch

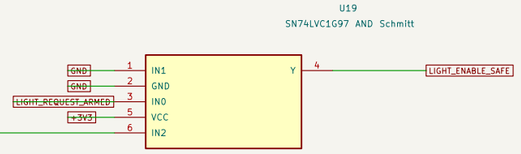
Title: Controller

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 2/20

POWER SEQUENCE

SUPPLY QUALIFICATION / HARDWARE LIGHTING INHIBIT

U19 SCHMITT AND: IN1=0, Y=READY AND IN0.
IN0 is U5 pin11: LIGHT_ENABLE AND physical ARM.
SAFE drives U13 bias, U14 SHDN, PCA OE and spot PWM gates.



U18 monitors +3V3: 3.07 V nominal falling threshold.
CT intentionally open: 12–28 ms reset release delay.
R42 limits discharge from existing MCU_EN capacitor C1.
MCU_EN pullup R1, capacitor C1 and manual S1 are on controller.

READY also feeds USB R41/R39: independent of ARM.
Prototype timing and 0<V3V3<1.65 V behavior require measurement.
After reset: initialize outputs OFF, verify PCA state, require fresh enable.

ENGINEERING DRAFT – see release status before fabrication
Engineered Lighting

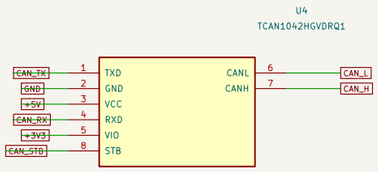
Sheet: /power_sequence/
File: power_sequence.kicad_sch

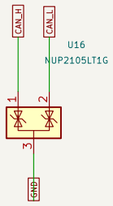
Title: Power Sequence

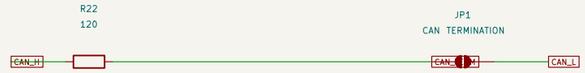
Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 3/20

CAN

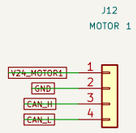
CAN: 5V transceiver supply / 3.3V logic interface.
Exactly two endpoint terminations; close JP1 only if this controller is an endpoint.

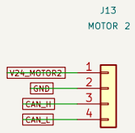






Motor connector: 1 = fused +24V, 2 = GND, 3 = CANH, 4 = CANL.
Unit-specific motor harness polarity must be verified before connection.





ENGINEERING DRAFT – see release status before fabrication
Engineered Lighting

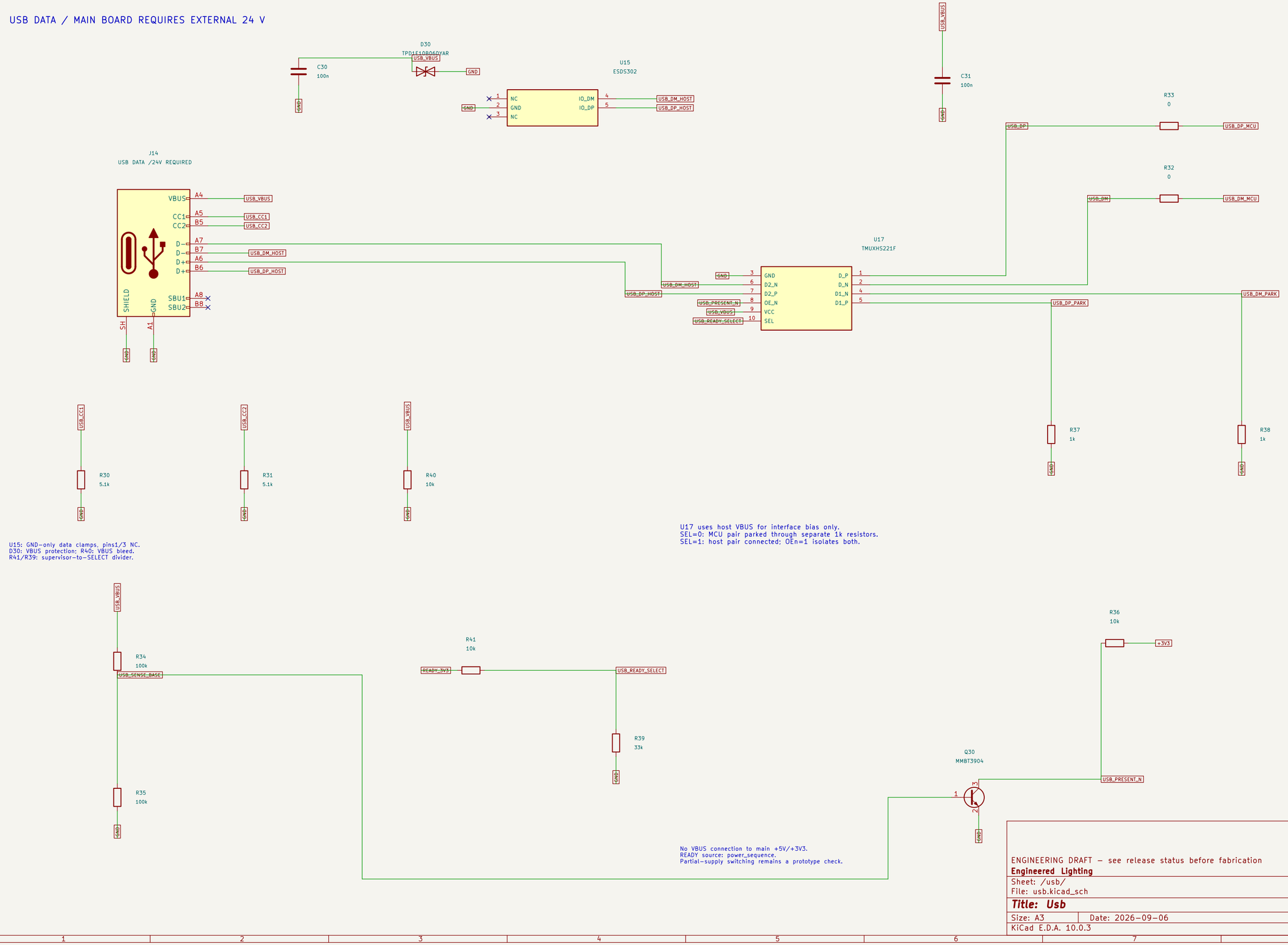
Sheet: /can/
File: can.kicad_sch

Title: Can

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 4/20

USB

USB DATA / MAIN BOARD REQUIRES EXTERNAL 24 V



ENGINEERING DRAFT – see release status before fabrication

Engineered Lighting

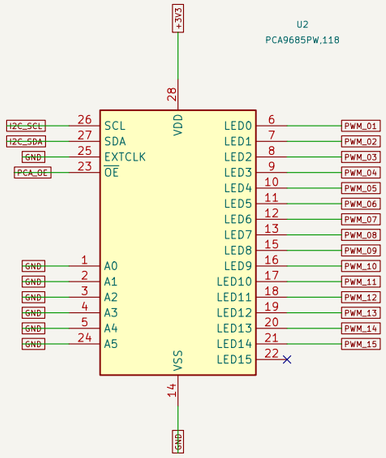
Sheet: /usb/
File: usb.kicad_sch

Title: Usb

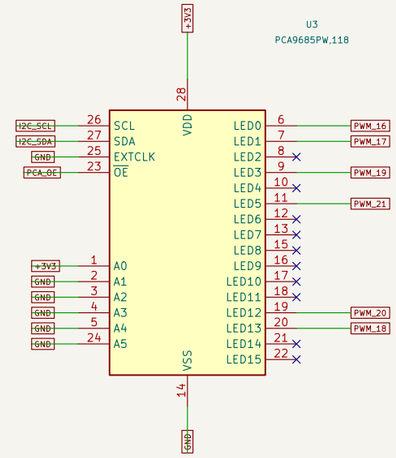
Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 5/20

PWM

U2 address 0x40 / zones 1–5



U3 address 0x41 / zones 6–7



24 outputs total: 21 here + 3 direct spotlight PWM.
OUTDRV=0, OUTNE=00; INVRT/duty encoding must be verified with outputs inhibited.

ENGINEERING DRAFT – see release status before fabrication

Engineered Lighting

Sheet: /pwm/
File: pwm.kicad_sch

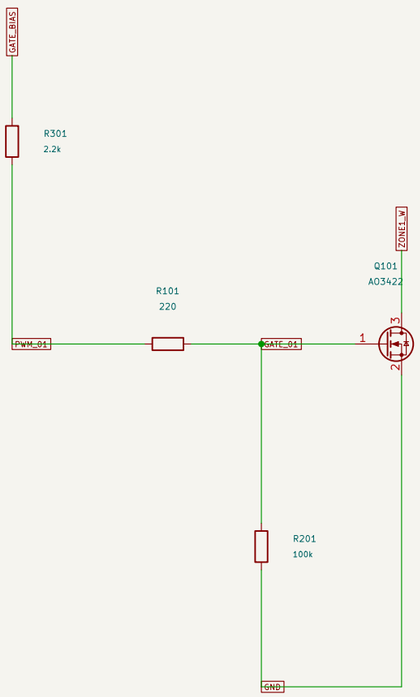
Title: Pwm

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 6/20

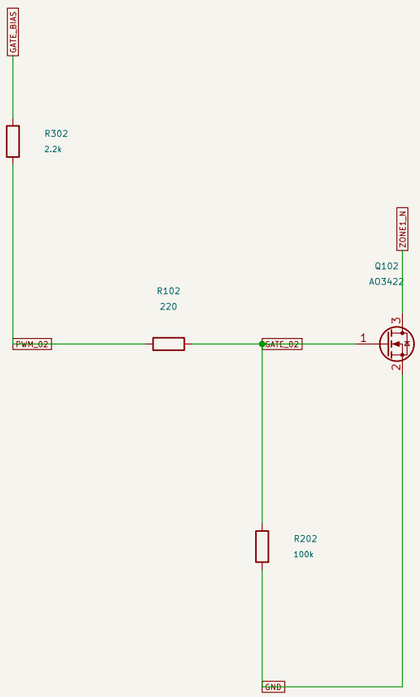
ZONE 1

24 V common positive; three independent low-side sinks.
Central J2 on central_led_interface: +24 V pins 16/17; W 18; N 19; C 20.

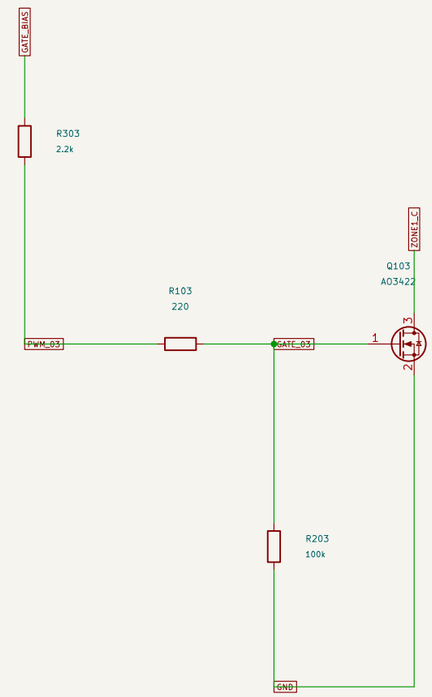
WARM / channel 1



NEUTRAL / channel 2



COOL / channel 3



GATE_BIAS is removed by U13 when LIGHT_ENABLE_SAFE is low.
PCA9685: open-drain; disabled output LOW. Firmware duty encoding requires verification.

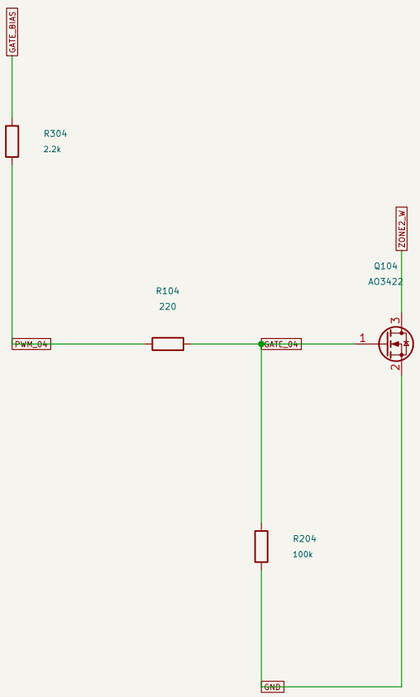
ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting

Sheet: /zone_1/		
File: zone_1.kicad_sch		
Title: Zone 1		
Size: A3	Date: 2026-09-08	**Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3		Id: 7/20

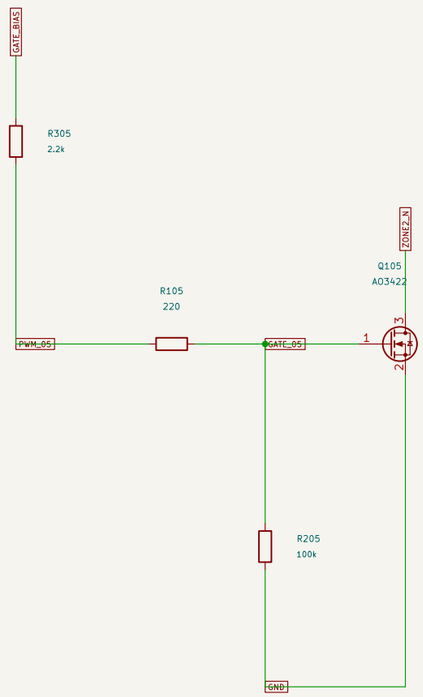
ZONE 2

24 V common positive; three independent low-side sinks.
Central J2 on central_led_interface: +24 V pins 21/22; W 23; N 24; C 25.

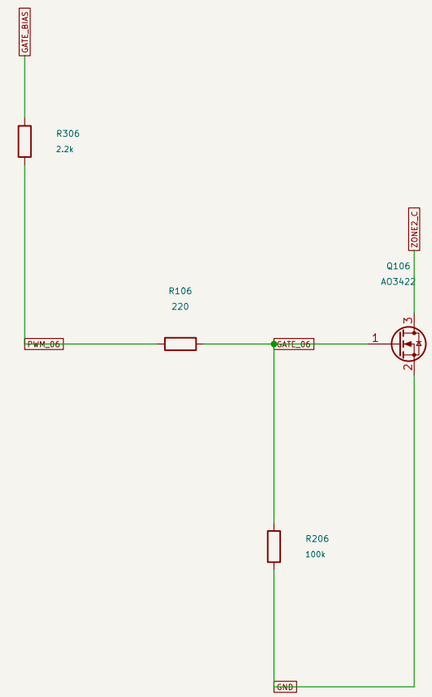
WARM / channel 4



NEUTRAL / channel 5



COOL / channel 6



GATE_BIAS is removed by U13 when LIGHT_ENABLE_SAFE is low.
PCA9685: open-drain; disabled output LOW. Firmware duty encoding requires verification.

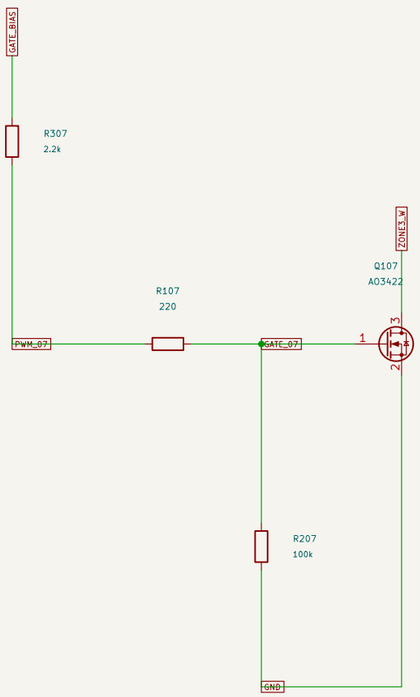
ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting

Sheet: /zone_2/		
File: zone_2.kicad_sch		
Title: Zone 2		
Size: A3	Date: 2026-09-08	**Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3		Id: 8/20

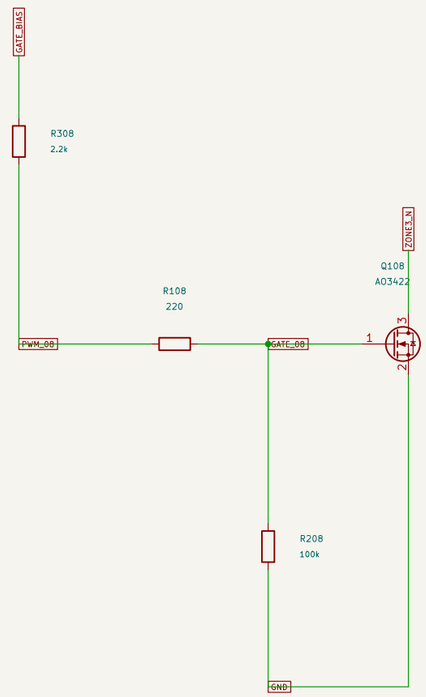
ZONE 3

24 V common positive; three independent low-side sinks.
Central J2 on central_led_interface: +24 V pins 26/27; W 28; N 29; C 30.

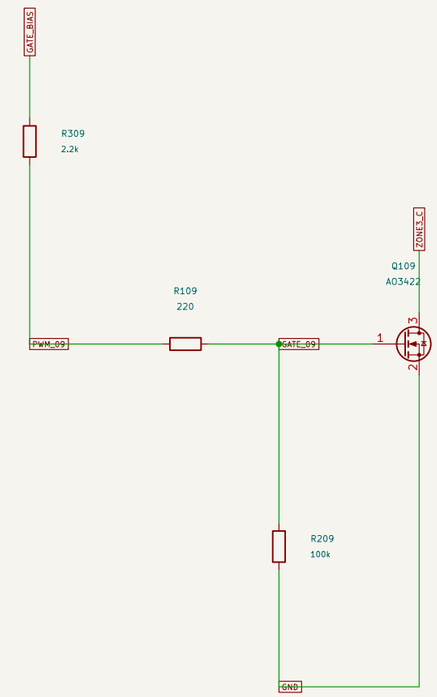
WARM / channel 7



NEUTRAL / channel 8



COOL / channel 9



GATE_BIAS is removed by U13 when LIGHT_ENABLE_SAFE is low.
PCA9685: open-drain; disabled output LOW. Firmware duty encoding requires verification.

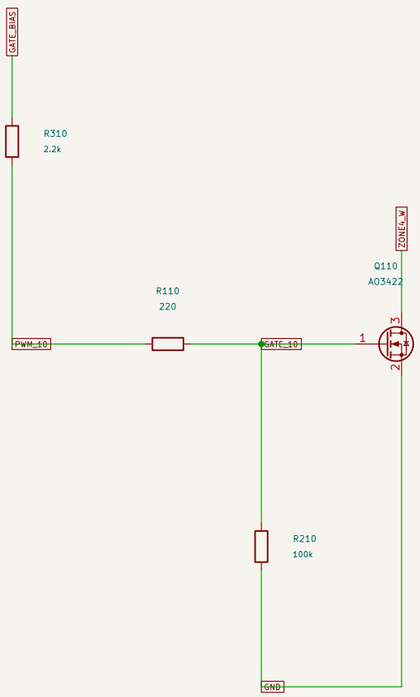
ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting

Sheet: /zone_3/		
File: zone_3.kicad_sch		
Title: Zone 3		
Size: A3	Date: 2026-09-08	**Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3		Id: 9/20

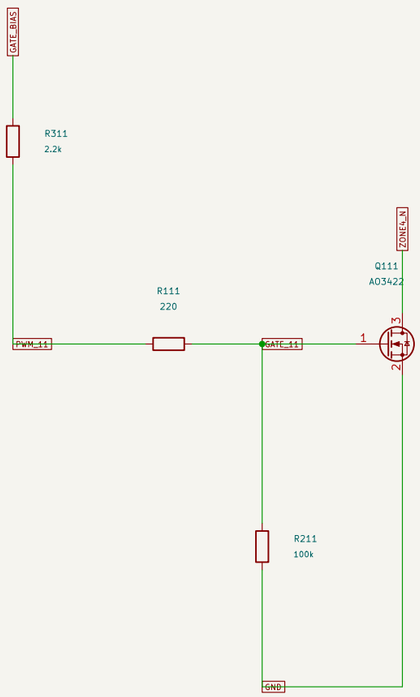
ZONE 4

24 V common positive; three independent low-side sinks.
Central J2 on central_led_interface: +24 V pins 1/2; W 3; N 4; C 5.

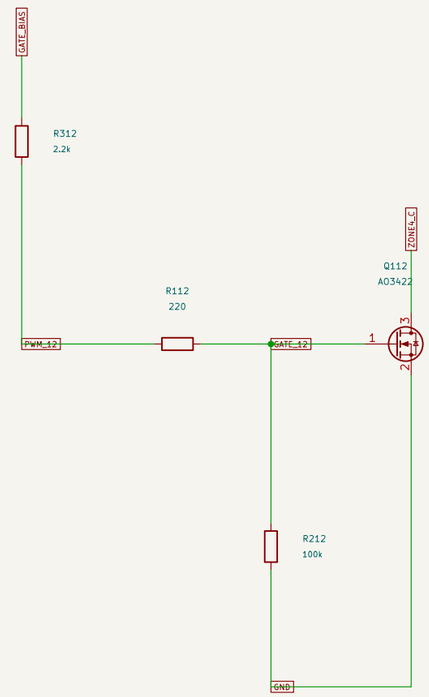
WARM / channel 10



NEUTRAL / channel 11



COOL / channel 12



GATE_BIAS is removed by U13 when LIGHT_ENABLE_SAFE is low.
PCA9685: open-drain; disabled output LOW. Firmware duty encoding requires verification.

ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting

Sheet: /zone_4/
File: zone_4.kicad_sch

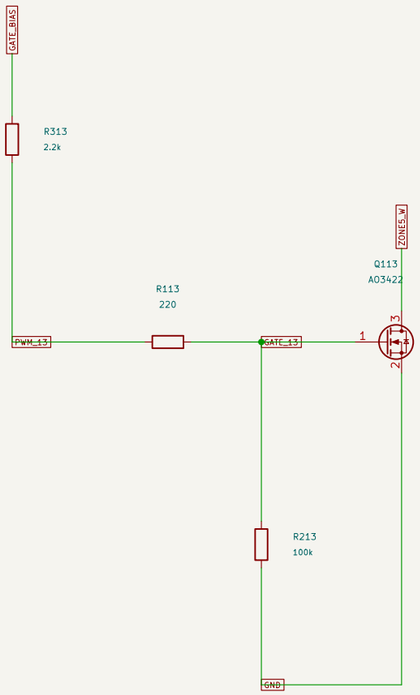
Title: Zone 4

Size: A3	Date: 2026-09-08	**Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3		Id: 10/20

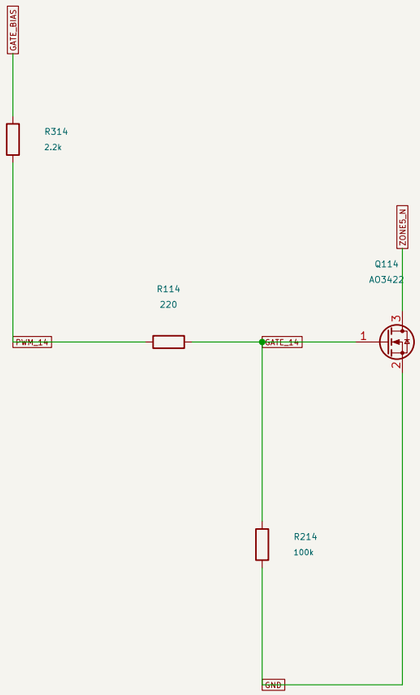
ZONE 5

24 V common positive; three independent low-side sinks.
Central J2 on central_led_interface: +24 V pins 6/7; W 8; N 9; C 10.

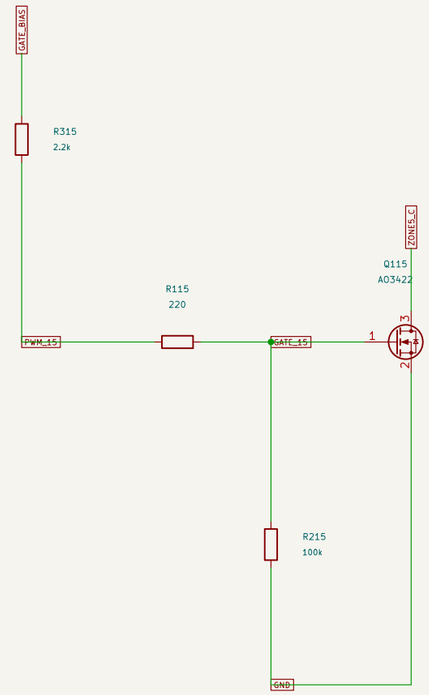
WARM / channel 13



NEUTRAL / channel 14



COOL / channel 15



GATE_BIAS is removed by U13 when LIGHT_ENABLE_SAFE is low.
PCA9685: open-drain; disabled output LOW. Firmware duty encoding requires verification.

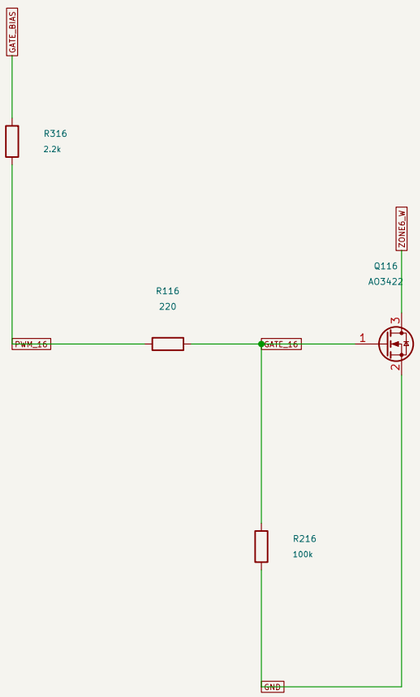
ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting

Sheet: /zone_5/		
File: zone_5.kicad_sch		
Title: Zone 5		
Size: A3	Date: 2026-09-08	**Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3		Id: 11/20

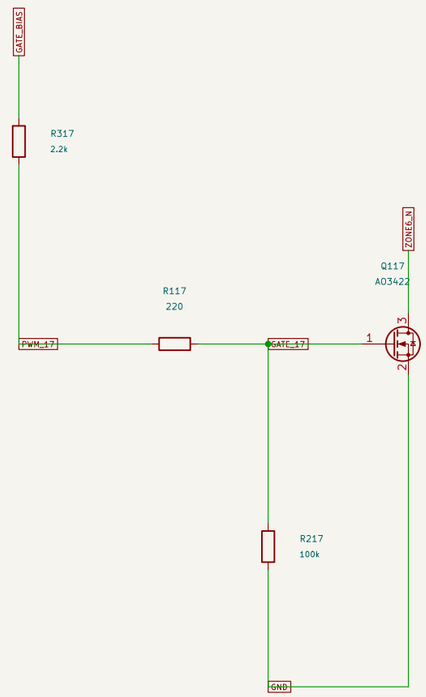
ZONE 6

24 V common positive; three independent low-side sinks.
Central J2 on central_led_interface: +24 V pins 11/12; W 13; N 14; C 15.

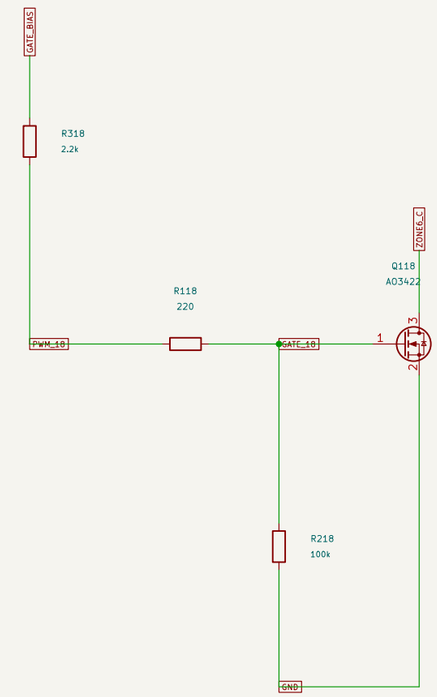
WARM / channel 16



NEUTRAL / channel 17



COOL / channel 18



GATE_BIAS is removed by U13 when LIGHT_ENABLE_SAFE is low.
PCA9685: open-drain; disabled output LOW. Firmware duty encoding requires verification.

ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting

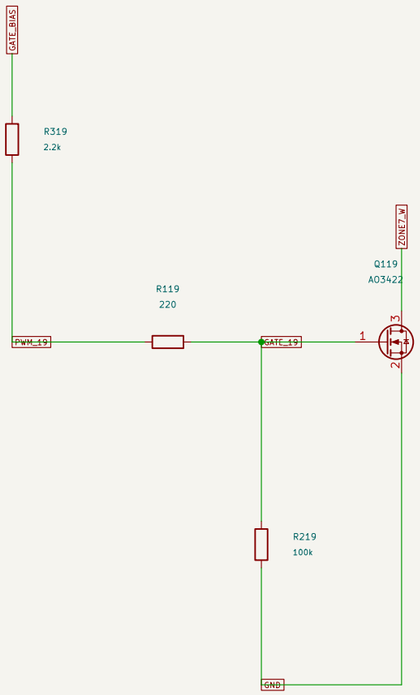
Sheet: /zone_6/		
File: zone_6.kicad_sch		
Title: Zone 6		
Size: A3	Date: 2026-09-08	**Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3		Id: 12/20

ZONE 7

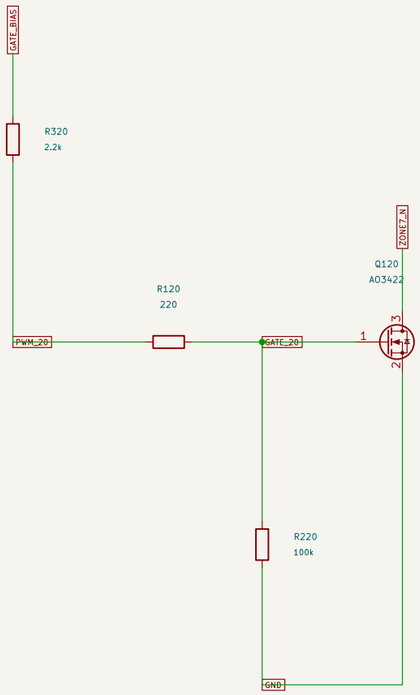
24 V common positive; three independent low-side sinks.
Connector poles: 1 = fused +24 V, 2 = W, 3 = N, 4 = C.

J8
ZONE 7

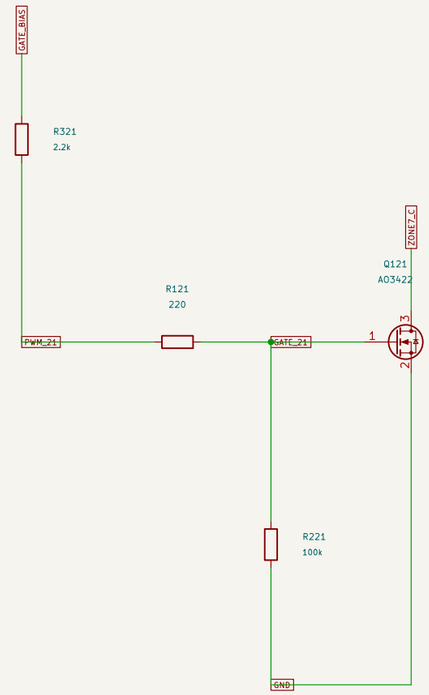
WARM / channel 19



NEUTRAL / channel 20



COOL / channel 21



GATE_BIAS is removed by U13 when LIGHT_ENABLE_SAFE is low.
PCA9685: open-drain; disabled output LOW. Firmware duty encoding requires verification.

ENGINEERING DRAFT – see release status before fabrication
Engineered Lighting

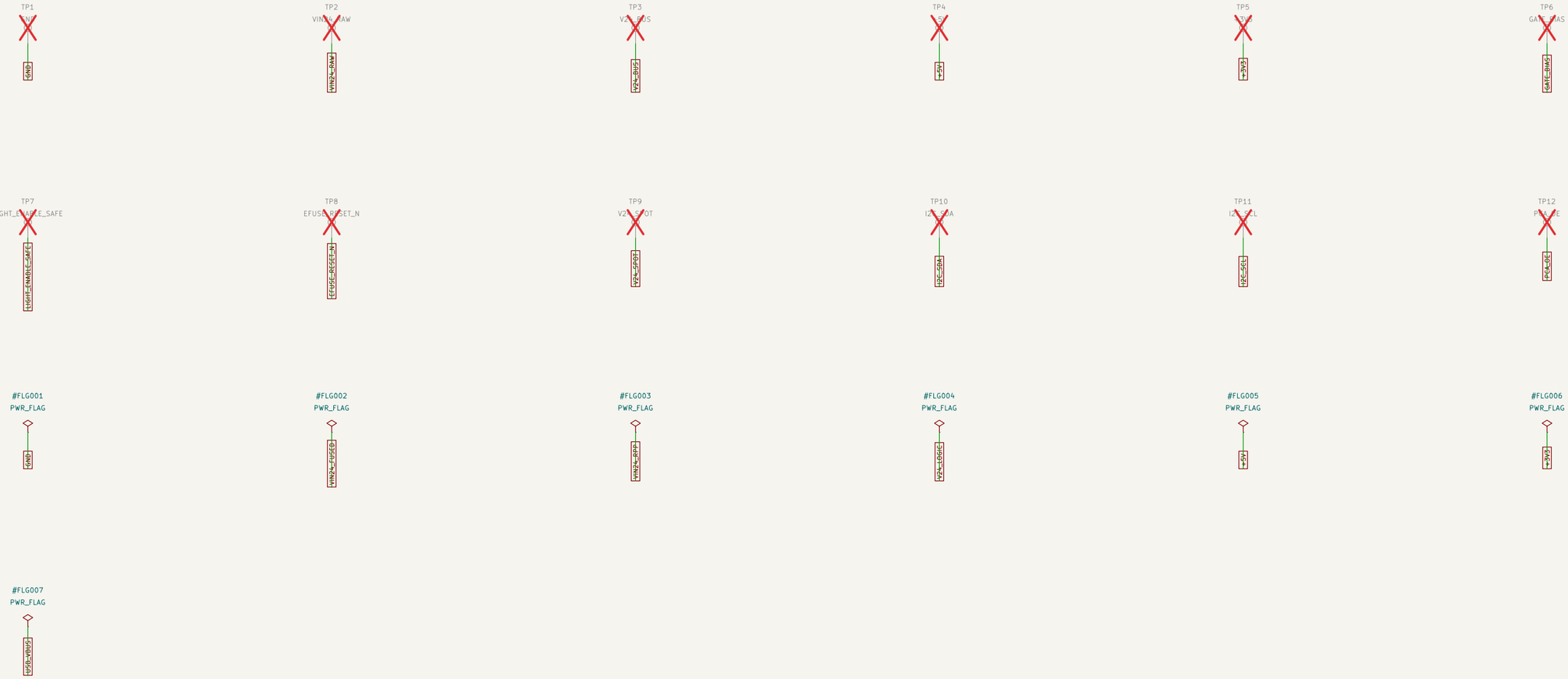
Sheet: /zone_7/
File: zone_7.kicad_sch

Title: Zone 7

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 13/20

TEST

COPPER TEST POINTS / POWER-FLAG ANNOTATIONS
Physical ARM must remain open during first power checks.



ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting

Sheet: /test/
File: test.kicad_sch

Title: Test

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 14/20

POWER 1

INPUT / REVERSE PROTECTION / MAIN eFUSE

F1
6.3A backup fuse

Q500
100V reverse blocking MOSFET

U12
24V input eFuse / 4.5A nominal

C504
1000uF 50V low ESR

J1 is on power_2. TVS input return is GND.
U12 nominal current limit 4.5 A; prototype operating target <= 4.0 A.

Q501
fast reverse gate pull-down

Threshold / status / startup components

D500
SMBJ33CA 33V bidirectional TVS

R500
4.02k

R501
140k

R502
10k

R503
210k

R504
10k

R505
165k

R506
10k

R507
10k

R508
10k

R509
10k

C500
100nF 100V X7R

C501
1uF 100V X7R

C502
100nF 100V X7R

C503
100nF 100V X7R

C505
100nF 100V X7R

FUSED DISTRIBUTION: motors / ambient zones / logic

F2
1A motor branch fuse

F3
1A motor branch fuse

F4
0.75A ambient zone fuse

F5
0.75A ambient zone fuse

F6
0.75A ambient zone fuse

F7
0.75A ambient zone fuse

F8
0.75A ambient zone fuse

F9
0.75A ambient zone fuse

F10
0.75A ambient zone fuse

F11
0.5A logic branch fuse

ENGINEERING DRAFT – see release status before fabrication
Engineered Lighting

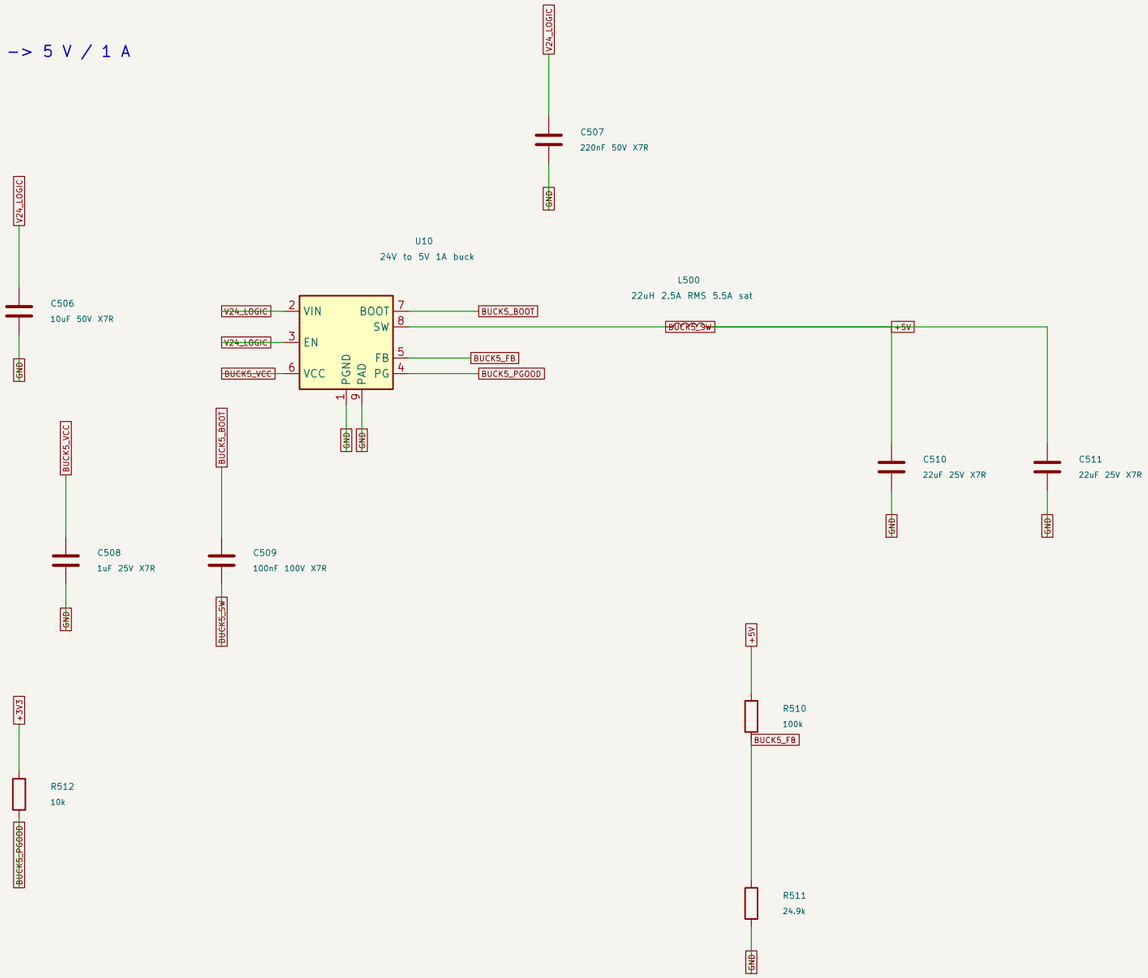
Sheet: /power_1/
File: power_1.kicad_sch

Title: Power 1

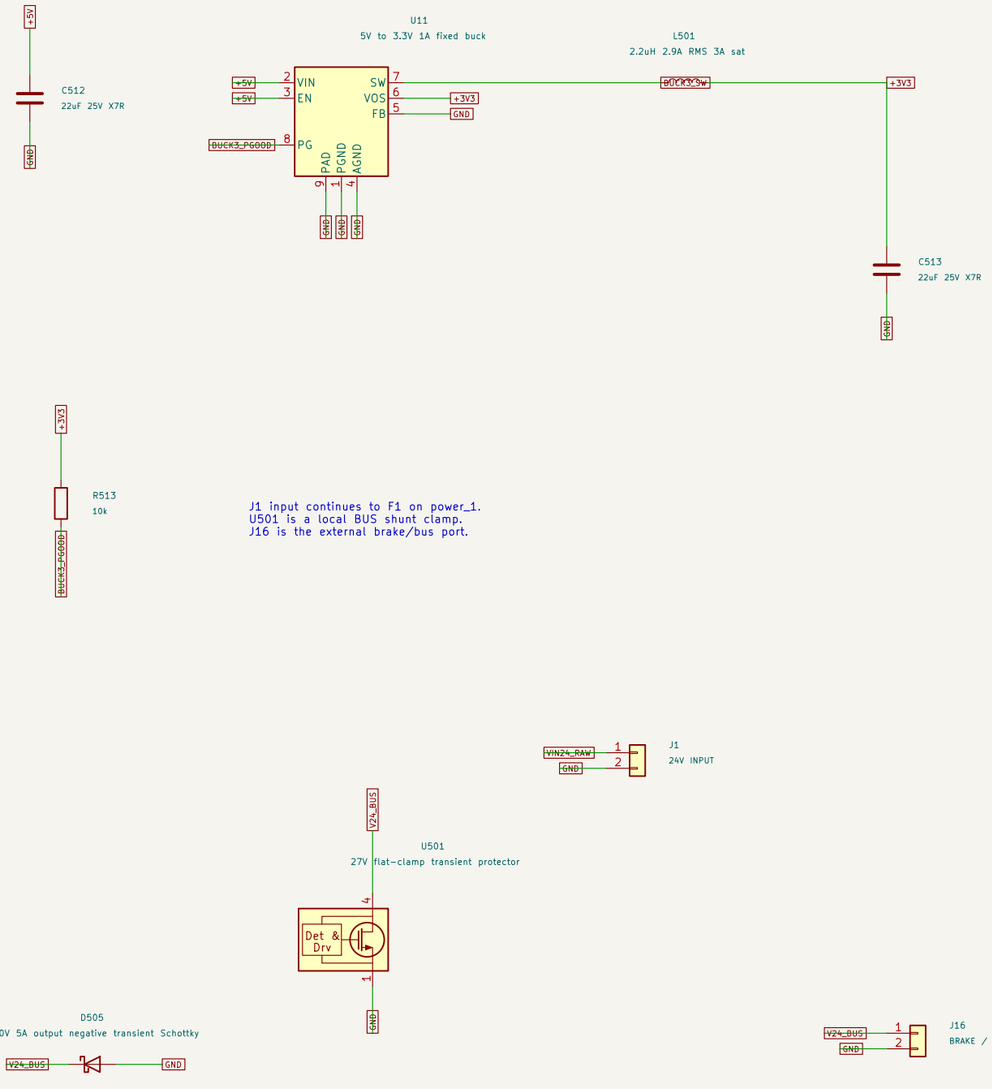
Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 15/20

POWER 2

24 V -> 5 V / 1 A

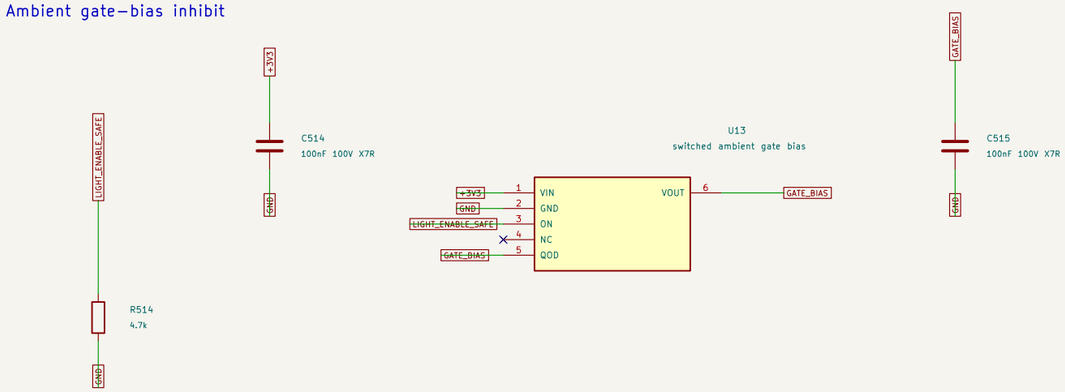


5 V -> 3.3 V / 1 A



J1 input continues to F1 on power_1.
U501 is a local BUS shunt clamp.
J16 is the external brake/bus port.

Ambient gate-bias inhibit



ENGINEERING DRAFT — see release status before fabrication

Engineered Lighting

Sheet: /power_2/
File: power_2.kicad_sch

Title: Power 2

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 16/20

SPOT 1

INDEPENDENT SPOT SUPPLY INHIBIT / 0.494 A NOMINAL

U14
spot branch gated eFuse 0.494A nominal

V24_BUS	1	IN	IMON 10 → SPOT_EFUSE_IMON
V24_BUS	2	IN	FLT 14 → SPOT_EFUSE_FLT_N
SPOT_RTN	3	UVLO	OUT 15
	4	NC	OUT 16 → V24_SPOT
SPOT_EFUSE_OVP	5	OVP	
SPOT_EFUSE_MODE	6	MODE	
LIGHT_ENABLE_SAFE	7	SHDN	
SPOT_RTN	8	RTN	
GND	9	GND	
SPOT_EFUSE_ILIM	11	ILIM	
SPOT_EFUSE_DVDT	12	dVdt	
	13	NC	
SPOT_RTN	17	RTN_EP	

V24_BUS → C517 100nF 100V X7R → GND

SPOT_EFUSE_ILIM → R515 24.3k → SPOT_EFUSE_DVDT → C516 47nF 50V X7R → SPOT_EFUSE_IMON → R519 10k → SPOT_RTN

SPOT_EFUSE_MODE → R516 402k → SPOT_RTN

V24_BUS → R517 210k → SPOT_EFUSE_OVP → R518 10k → SPOT_RTN

V24_SPOT → C518 100nF 100V X7R → V24_SPOT_GND → R521 47k → GND

D501
60V output negative transient Schottky
V24_SPOT → GND

+3V3 → R520 10k → SPOT_EFUSE_FLT_N

SPOT_RTN belongs to U14: do not join it to GND. Stored charge remains after inhibition.

CH3 diode/input capacitors continue on spot_2.

SPOT 1 / 333 mA nominal

V24_SPOT → C519 10uF 50V X7R → GND

V24_SPOT → C520 10uF 50V X7R → GND

U7
333mA spotlight CC driver

CTRL, VIN, SET, GND, SW

V24_SPOT → R523 0.300ohm 1% 0.125W → SPOT1_LED_PLUS

V24_SPOT → D502 60V 1A flyback Schottky → SPOT1_LED_MINUS

SPOT1_CTRL → R526 910 → GND

SPOT1_SW → L502 220uH +/-20%, .6A RMS .7A saturation → SPOT1_LED_MINUS

Paired LED output -> J9 pins 1/2 / spot_2

SPOT 2 / 333 mA nominal

V24_SPOT → C521 10uF 50V X7R → GND

V24_SPOT → C522 10uF 50V X7R → GND

U8
333mA spotlight CC driver

CTRL, VIN, SET, GND, SW

V24_SPOT → R524 0.300ohm 1% 0.125W → SPOT2_LED_PLUS

V24_SPOT → D503 60V 1A flyback Schottky → SPOT2_LED_MINUS

SPOT2_CTRL → R527 910 → GND

SPOT2_SW → L503 220uH +/-20%, .6A RMS .7A saturation → SPOT2_LED_MINUS

Paired LED output -> J9 pins 3/4 / spot_2

SPOT 3 / 333 mA nominal

V24_SPOT → C523 10uF 50V X7R → GND

V24_SPOT → C524 10uF 50V X7R → GND

U9
333mA spotlight CC driver

CTRL, VIN, SET, GND, SW

V24_SPOT → R525 0.300ohm 1% 0.125W → SPOT3_LED_PLUS

SPOT3_CTRL → R528 910 → GND

SPOT3_SW → L504 220uH +/-20%, .6A RMS .7A saturation → SPOT3_LED_MINUS

Paired LED output -> J9 pins 5/6 / spot_2

ENGINEERING DRAFT – see release status before fabrication

Engineered Lighting

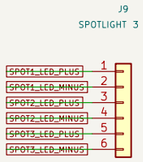
Sheet: /spot_1/
File: spot_1.kicad_sch

Title: Spot 1

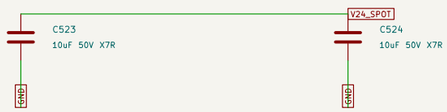
Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 17/20

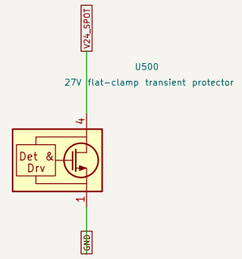
SPOT 2

J9: 1/2 = SPOT1 +/−, 3/4 = SPOT2 +/−, 5/6 = SPOT3 +/−.
All three LED pairs remain independent; LED− is not GND.
The wire service loop reaches the static arm flex; J13 separately carries tilt power and CAN.



CH3 current loop continuation from U9 on spot_1





U500 local spotlight-rail shunt clamp.
Pulse limits do not establish continuous braking.

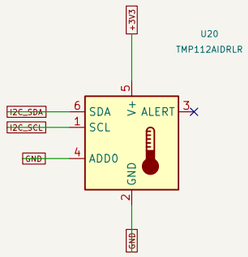
ENGINEERING DRAFT – see release status before fabrication
Engineered Lighting

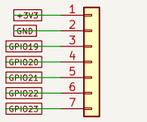
Sheet: /spot_2/
File: spot_2.kicad_sch

Title: Spot 2

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 18/20

MONITOR EXPANSION





ENGINEERING DRAFT — see release status before fabrication

Engineered Lighting

Sheet: /monitor_expansion/
File: monitor_expansion.kicad_sch

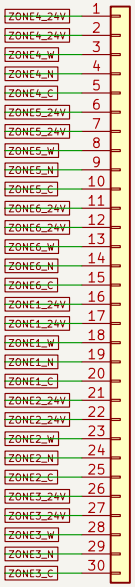
Title: Monitor Expansion

Size: A3	Date: 2026-09-06	**Rev: A draft**
KiCad E.D.A. 10.0.3		Id: 19/20

SIX ZONES / ONE LOCKING FLEX CONNECTION

J2 mates directly to upper LED flex J100.
30 contacts carry 24 independent electrical nets.
Fused positive rails remain separate for every zone.

J2
2005280300 / 6-ZONE FLEX



PIN BLOCKS: 4 / 5 / 6 / 1 / 2 / 3
Within each block: +24 V, +24 V, W, N, C
Duplicate positive contacts connect ONLY within that zone.
No common ground contact; these are switched LED returns.

MATING: Molex 2005280300, bottom contact / Front Flip.
Upper-flex contacts are B.Cu; reinforcement is FRONT.
Native flex front view, tip up: pin 1 LEFT.
Looking directly at gold, tip up: pin 1 RIGHT.
Gold faces main PCB when inserted.
Mate only with power disconnected; provide strain relief.

Finished insertion thickness 0.30 +/-0.05 mm, all layers included.
Fingers: gold >=0.1 um over nickel 1-5 um; no solder coating.
Tail dimensional and stack acceptance required from fabricator.
See MATING-TAIL-CONTRACT.json and fabrication drawing.

ENGINEERING DRAFT — see release status before fabrication
Engineered Lighting
Sheet: /central_led_interface/
File: central_led_interface.kicad_sch
Title: Central six-zone LED flex interface
Size: A4 | Date: 2026-09-08 | **Rev: LIGHT v0.2 candidate**
KiCad E.D.A. 10.0.3 | Id: 20/20